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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,913	05/07/2002	Michael O. Thompson	3672-0144P	8909

2292 7590 03/23/2007

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EXAMINER	
HUR, JUNG H	
ART UNIT	PAPER NUMBER
2824	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/23/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/23/2007.

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mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/088,913	THOMPSON ET AL.	
	Examiner	Art Unit	
	Jung (John) H. Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2006 and 23 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *6-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submissions filed on 27 December 2006 and 23 February 2007 have been entered.

Amendment

2. Acknowledgment is made of applicant's Amendments, filed 27 December 2006 and 23 February 2007. The changes and remarks disclosed therein have been considered.

Claims 17 and 18 have been added by Amendment. Therefore, claims 1-18 are pending in the application.

Claims 6-11 remain withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected invention and species, there being no allowable generic or linking claim.

Specification

3. Claims 6-9 are objected to because of the following informalities:

The status of claims 6-9 should be --Withdrawn--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 13, 14, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709).

Regarding claims 1, 13 and 17, Kuroda, for example in Figs. 1 and 2, discloses a non-volatile passive matrix memory device comprising ferroelectric memory cells (for example, C0-C7 in Fig. 2); word lines (for example, W00-W07 in Fig. 2) and bit lines (for example, D0-D7 in Fig. 2) that are orthogonal to each other, where each memory cell is at all times in physical contact with a word line and a bit line (for example, in Fig. 2, the memory cell C0 is directly connected to or is directly contacting the word line W00 and the bit line D0; i.e., a transistor is not used to make a connection or contact to a word line or a bit line); the word lines divided into a number of segments (for example, BLOCK (0,0) through BLOCK (0,7) in Fig. 1), each segment comprising and being defined by a plurality of adjoining bit lines (for example, D0-D7 for BLOCK (1,0)); each word line in a segment is differentiated based on the position of the word line within the segment (i.e., in different row positions), each word line in the segment being adjoined to a separate bit line (i.e., in a matrix structure); a plurality of sensing means (for example, SA in WRC0-WRC7), each being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line (see, for example, column 12, lines 42-54).

However, Kuroda does not disclose means for connecting each separate bit line assigned to a segment with a different associated sensing means, such that a world line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment.

Clemons, for example in Figs. 2 and 3, discloses a means (for example, via T200-T203 controlled by BYTE BLOCK DECODER) for connecting each separate bit line (for example, bit lines for columns C11-C14) assigned to a segment (for example, BYTE BLOCK 1, when selected) with a different associated sensing means (for example, SA1-SA4 via I/O SWITCHES in Fig. 3), such that the world line of the same position within each segment is selected within each segment (i.e., for example, a selected word line within BYTE BLOCK 1), each word line of the same position being sensed at the same time by said respective different associated sensing means (for example, SA1-SA4 via I/O SWITCHES in Fig. 3), thus enabling simultaneous connection of all memory cells (for example, M111 - M114) assigned to a word line (for example, R1) on a segment (for example, BYTE BLOCK 1) for readout via the corresponding bit lines (for example, bit lines for columns C11 - C14) of the segment.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Kuroda by incorporating the means of Clemons for connecting each bit line assigned to a segment with an associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, as an equivalent alternative means for

segmenting and simultaneously accessing a byte (or a word or other widths of bits) of information from the memory (compare with Fig. 1 of Clemons, which is similar to the configuration of Kuroda), for the purpose of having a ferroelectric memory organization that provides for improved utilization of spare columns, while allowing for subdivision of the memory into portions (see Clemons column 3, lines 40-43).

Regarding claims 14 and 16, the above Kuroda/Clemons combination further discloses that the number of sensing means is equal to the number of bit lines within each segment (for example, Figs. 2 and 3 of Clemons, as applied to the above combination, show 4 sensing means SA1-SA4 for 4 bit lines within each segment or BYTE BLOCK), where each segment contains the same number of bit lines (for example, 4 bit lines in each BYTE BLOCK in Fig. 2 of Clemons), such that each bit line in each segment (when selected) is sensed at a different sensing means (via corresponding SA1-SA4 in Fig. 3 of Clemons).

6. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709) as applied to claim 1 above, and further in view of Dierke (U.S. Pat. No. 5,734,615).

Regarding claim 2, the combination of Kuroda and Clemons discloses a non-volatile passive matrix memory device as in claim 1 above, with the exception of the simultaneous connection of each bit line of a segment with the associated sensing means during addressing is accomplished by multiplexers.

Dierke, for example in Fig. 7, discloses multiplexers (42-0' through 42-7') for simultaneously connecting (since multiplexers are commonly controlled) each bit line of a segment (three segments defined by BIT 0-7, BIT 8-15 and BIT 16-23) with an associated sensing means (at the output of each multiplexer).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the multiplexing means of Dierke for the multiplexing means of Clemons, since both means are equivalent for simultaneously connecting bit lines of a segment with an associated sensing means, for the purpose of having a ferroelectric memory organization that provides for improved utilization of spare columns, while allowing for subdivision of the memory into portions (see Clemons column 3, lines 40-43), and the selection of these equivalents would be within the level of ordinary skill in the art.

Regarding claims 3-5, the above Kuroda/Clemons/Dierke combination further discloses that the number of multiplexers corresponds to the largest number of bit lines defining a segment (in Fig. 7 of Dierke, eight bit lines per segment; when adapted for Clemons with four multiplexers; see Clemons, Fig. 2), each bit line of a segment being connected with a specific multiplexer (see Dierke, Fig. 7 in which BIT 0-7, for example, are connected to the respective multiplexers); wherein the output of each multiplexer is connected with a signal sensing means (inherent in Dierke, Fig. 7; SA1-SA4 in Fig. 3 of Clemons); wherein the signal sensing means is a sense amplifier (SA1-SA4 in Fig. 3 of Clemons).

7. Claims 12, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709) as applied to claim 1, 14 and 17 above, and further in view of Seyyedy (U.S. Pat. No. 5,969,380).

Regarding claims 12, 15 and 18, the combination of Kuroda and Clemons discloses a non-volatile passive matrix memory device as in claims 1, 14 and 17 above, with the exception of a volumetric data storage apparatus with a plurality of stacked layers, each layer comprising one of said non-volatile passive matrix memory devices. Seyyedy, for example in Figs. 1 and 2, discloses a ferroelectric volumetric data storage apparatus with a plurality of stacked layers (for example, four layers in Fig. 1 and three layers in Fig. 2), each layer comprising one of non-volatile passive matrix memory devices (planar ferroelectric memory arrays). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to stack a plurality of devices (as discloses in the above combination of Kuroda and Clemons) in a volumetric data storage apparatus, as in Seyyedy, for the purpose of increasing the density of memory cells over a given substrate area.

Response to Arguments

8. Applicant's arguments filed 27 December 2006 have been fully considered but they are not persuasive.

Applicant, starting in the middle of page 13, argues that, in Clemons, "[t]he addressing of the voltage on the bit lines to specific sense amplifiers is not based on segmentation of the word lines," and that "[i]n segmenting based on the word lines, as in embodiments of the present invention, all bit lines across the entire array associated with those word line segmentations can

be sent simultaneously at the associated sensing means" and that Clemons is not "segmented based on the word lines" but "relies on accessing via the transistors for a given bock."

In response, it is noted that, in Figs. 5 and 6 of the instant application (which are understood to be the "embodiments of the present invention" mentioned above), all bit lines across the entire array associated with those word line segmentations (S_1-S_q) are "sent simultaneously at" the associated sensing means (26_1-26_k) through multiplexers (Fig. 5) or pass gates (Fig. 6); however, only the bit lines of a selected segment (via multiplexers or pass gates) are sensed simultaneously by the sensing means (26_1-26_k), which is similar to the configuration in Figs. 2 and 3 of Clemons.

Applicant, in the 2nd and 3rd full paragraphs on page 14, argues that "each of references Clemons and Kuroda teach an active matrix memory, which is contrary to the passive memory of the present invention," and that "[i]n active matrices all memory cells are not permanently in physical contact with the electrode as each memory requires the activation of a transistor to obtain physical electrode contact."

In response, it is noted that Kuroda does teach a passive matrix memory with segmented word lines in which bit lines and word lines which form the memory cells are in physical contact with each other. See, for example, Fig. 2 of Kuroda which shows each memory cell in physical contact with one of the word lines (W00-W07) and one of the bit lines (D0-D7), i.e., not through a transistor or a switching element. Further, Clemons was cited as a secondary reference that discloses a means for simultaneously sensing all the bit lines in a word line segment.

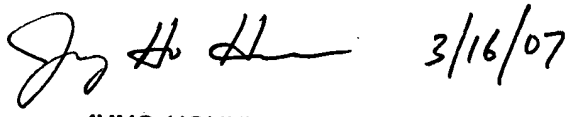
Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) H. Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh



3/16/07

JUNG (JOHN) H. HUR
PRIMARY PATENT EXAMINER